Patent claims

1. The driving scheme for the LCD electrooptic element with alternating square-wave electric signals, the amplitude of which can vary between different electric levels so that the optimum dynamics of the electrooptic response is assured, characterized in that the changing of the polarity of the electric driving signals is controlled by the integrator, which integrates the potential difference between the electrodes of the LCD electrooptic switching element so that it keeps the value of the time integral I_{nt} of the driving voltage within the predetermined interval ($V_{C1} \leq I_{nt} \leq V_{C2}$), determining the time interval for the polarity change of the electric driving signals as well as allowing for the complete annihilation of the long-term DC component of the electric driving signals for the LCD electrooptic switching element.

2. The driving scheme for the LCD electrooptic switching element as claimed in claim 1, characterized in that in the case that the amplitude of the of the electric driving signals for the said switching element is changing in time, the said predetermined interval (V_{C1}, V_{C2}) for the time integral I_{nt} of the potential difference between the electrodes of the LCD electrooptic switching element is synchronously with the first even change of the polarity of the said electric driving signals, which corresponds to a completion of the DC driving voltage compensation cycle and follows the amplitude change, adjusted according to the electric driving signal amplitude variation in such a way that the time interval of the electric driving signals polarity changes remains as constant as possible.

3. The electronic circuitry for the implementation of the driving scheme of claim 1, characterized in that the electric driving signals on the electrodes (2) and (3) of the LCD electrooptic switching element (1) are connected to the difference inputs (4) and (5) of the differential amplifier (6), the output signal (7) of which is connected to the input (8) of the integrator (9) and

that the output signal (10) of the integrator (9) is connected to the comparator inputs (12) and (22) of the comparators (13) and (20), the reference inputs (11) and (21) of which are connected to the electric potentials V_{C2} and V_{C1} respectively, while the signals, generated at the outputs (14) and (23) of the comparators (13) and (20), enable the control over the logic control signals for the LCD electrooptic switching element (1) via the "set/reset" inputs (16) and (15) of the control "flip/flop" circuit (17) so that the electric driving signals for each of the electrodes of the LCD electrooptic switching element (1), generated at its outputs (18) and (19) are phase shifted by 180° (Q/ $\bar{Q}$) and

ART 34 AMDT

that these logic control signals are connected to the inputs (39) and (40) of the voltage translator (36), which transforms them into the driving signals for the LCD electrooptic switching element (1) at its outputs (37) and (38) connected to the control electrodes (2) and (3) of the LCD electrooptic switching element (1), the amplitude of these driving signals being determined by the voltage level V_{LCD}, which is connected to the control input (41) of the voltage translator (36) and

that the said electronic driving circuitry can be optionally complemented with the electronic circuitry for the reduction of the time-interval variations of the polarity change of the electric driving signals for the LCD electrooptic switching element (1)

4. The electronic circuitry for the implementation of the driving scheme of claims 1 and 2 as claimed in claim 3, characterized in that it reduces the time-interval variations of the polarity change of the electric driving signals by means of using the additional analog switch (24) that selects between the voltage levels V_{S1} and V_{S2}, connected to the inputs (27) and (28) of the said analogue switch so that it changes the reference voltage V_{C1} at its output (25), connected to the reference input (21) of the comparator (20) and

that the selection of the reference voltage is made synchronously with the adequately selected driving signal for the LCD electrooptic switching element (1) and according to the signal given by the sensor element (35) so that the signal, which is generated by the sensor (35) at its output (34), connected to the synchronization input (31), synchronizes the logic control circuitry (30) in such a way that the logic signal at its output (32), connected to the control input (26) of the analogue switch (24), controls the said analogue switch in such a way that it selects the voltage level V_{C1} at its output (25), connected to the reference input (21) of the comparator (20), so that the time-interval variations of the polarity change of the electric driving signals, controlled by the comparator (20), are as small as possible.

5. The electronic circuitry for the implementation of the driving scheme of claim 1, characterized in that the electric driving signals on the electrodes (2) and (3) of the LCD electrooptic switching element (1) are connected to the inputs (49) and (50) of the analogue switch (48), the output signal (51) of which is connected to the input (8) of the integrator (9) and

that the output signal (10) of the integrator (9) is connected to the comparator input (56) of the comparator (54), the reference input (55) of which is connected to the electric potential V_C, while the signal generated at the output (57) of the comparator (54) enables the control of the logic driving signals for the LCD electrooptic switching element (1) via the input (16) of the control "flip/flop" switching circuit (17) so that the electric driving signals for each of the electrodes of the LCD electrooptic switching element (1), generated at its outputs (18) and (19) are phase shifted for 180° (Q/ $\bar{Q}$) and that at the same time the output (19) of the switching electronic circuitry (17) is connected to the control input (58) of the analog switch (48), selecting one of the driving electric voltages of the LCD electrooptic switching element (1) and that the output (57) of the comparator (54), is connected to the select input (61) of the analog switch (60), so that with every change of the polarity of the electric driving field between the electrodes of the LCD electrooptic switching element (1) the said analogue switch (60) switches for a short time its output (53), connected to the input (52) of the of the integrator (9), from its electrically floating input (62) to the adequately chosen constant electric potential, connected to its input (63), which results in resetting the integrator (9) to the initial state and

that the logic driving signals at the outputs (18) and (19) of the switching logic circuitry (17) are connected to the inputs (39) and (40) of the voltage translator (36) that transforms them on its outputs (37) and (38), connected to the electrodes (2) and (3) of the LCD electrooptic switching element (1), into the electric driving signals for the said LCD electrooptic switching element (1), the amplitude of which being determined by the electric voltage V_{LCD}, connected to the control input (41) of the voltage translator (36) and

that this electronic circuitry can be optionally complemented with the electronic circuitry for the reduction of the time-interval variations of the polarity-change of the electric driving signals for the LCD electrooptic switching element (1)

6. The electronic circuitry for the implementation of the driving scheme of claim 1, characterized in that the voltage output (43) of the analogue switch (42) which is apart from being connected to the input (41) of the voltage translator (36), connected also directly to the input (8) of the integrator (9) and

that the output signal (10) of the integrator (9) is connected to the comparator input (56) of the comparator (54), the reference input (55) of which is connected to the electric potential V_C, while the signal generated at the output (57) of the comparator (54) enables the control of the

ART 34 AMDT

22

logic driving signals for the LCD electrooptic switching element (1) via the input (16) of the control "flip/flop" switching circuit (17) so that the driving signals for each of the electrodes of the LCD electrooptic switching element (1), generated at its outputs (18) and (19) are phase shifted for 180° (Q/ $\bar{Q}$) and

that the output (57) of the comparator (54) is connected to the select input (61) of the analogue switch (60) so that with every change of the polarity of the electric driving field between the electrodes of the LCD electrooptic switching element (1) the said analogue switch (60) switches for a short time its output (53), which is connected to input (52) of integrator (10), from its electrically floating input (62) to the adequately chosen constant electric potential V_p, connected to its input (63), which results in resetting the integrator (9) to the initial state and

that the logic driving signals at the outputs (18) and (19) of the switching logic circuitry (17) are connected to the inputs (39) and (40) of the voltage translator (36) that transforms them on its outputs (37) and (38), connected to the electrodes (2) and (3) of the LCD electrooptic switching element (1), into the electric driving signals for the said LCD electrooptic switching element (1), the amplitude of which being determined by the electric voltage V_{LCD}, connected to the control input (41) of the voltage translator (36) and

that this electronic circuitry can be optionally complemented with the electronic circuitry for the reduction of the time-interval variations of the polarity-change of the electric driving signals for the LCD electrooptic switching element (1).

7. The electronic circuitry for the implementation of the driving scheme of claims 1 and 2 as claimed in claims 5 and 6, characterized in that it reduces the time-interval variations of the polarity change of the electric driving signals by using the additional analog switch (24), which selects between the voltage levels V_{S1} and V_{S2} connected to the inputs (27) and (28) of the said analog switch so that it changes the reference voltage V_C at its output (25) connected to the reference input (55) of the comparator (54) and

SUBA2 13/2

that the selection of the reference voltage is made according to the signal given by the sensor element (35) and synchronized with the appropriate electric driving signal for the LCD electrooptic switching element (1) so that the signal that is generated by the sensor (35) at its output (34), connected to the synchronization input (31), synchronizes the logic control circuitry (30), which through its output (32), connected to the control input (26) of the analogue switch

ART 34 AMDT

(24), controls the said analogue switch (24) in such a way that it selects the reference voltage V_c at its output (25), connected to the reference input (55) of the comparator (54), so that the time-interval variations of the polarity change of the electric driving signals, controlled by the comparator (54), are as small as possible.

SUB A27 B12

8. The electronic circuitry for the implementation of the driving scheme of claim 1 as claimed in claims 5 and 6, characterized in that the integration of the LCD electrooptic switching element driving signals is implemented by the periodic, sufficiently frequent, transfer of the charge proportional to the LCD electrooptic switching element driving voltage, into the integrating capacitor (110) by the transfer capacitor (101) and electronic analog switches (102) and (103), where the complete transfer of the charge from the transfer capacitor (101) into the integrating capacitor (110) is provided by two transistors of the opposite polarity (115) and (116) with base leads interconnected and emmitor leads interconnected.

9. The electronic circuitry for the implementation of the driving scheme of claim 1 as claimed in claims 5 and 6, characterized in that the comparation of the integral of the LCD control signals with the reference voltage V_c and the discharging of the integrating capacitor (110) is provided by two transistors of the opposite polarity (117) and (118), which have their base leads connected to the collector leads of the other transistor, while remaining emitter leads are connected to the integrating capacitor (110) and the output signal from the circuit is provided by additional NPN transistor (119).

ADD A37 B12